

THIN FILM TRANSISTOR PANEL FOR LIQUID CRYSTAL DISPLAY

ABSTRACT OF THE DISCLOSURE

5 A thin film transistor array panel is provided, which includes: a pair of first and second gate lines; a data line intersecting the gate lines in an insulating manner; a storage electrode line supplied with a common voltage; a pixel electrode formed in a pixel area defined by the intersections of the first and the second gate lines and the data line and including a plurality of subareas partitioned by cutouts; a direction control electrode formed in the pixel area and including a portion overlapping at least one of the cutouts; a first thin film transistor connected to the pixel electrode, the first signal line, and the third signal line; a second thin film transistor connected to the pixel electrode, the second signal line, and the third signal line; and a third thin film transistor connected to the direction control electrode, the second signal line, and the fourth signal line.

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